

Yum, Jung Hwan (J. H. Yum or J. Yum et al.)

To apply the job opportunity in the fields of microelectronic devices, oxide superconductor, optoelectronics, nano devices and laser system of electrical engineering

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EDUCATIONAL BACKGROUND

PhD in Electrical Engineering

Solid state & Plasma Quantum Electronics track, Electrical and Computer Engineering Department,
University of Texas at Austin
Period: August, 2006 – 2012. May

Master of Science in Electrical Engineering

Electrical Engineering Department, University of Southern California, Los Angeles, California
Period: January, 2005 – May, 2006

Bachelor of Science in Electrical Engineering

Korea University, Seoul, Korea
Period: March, 1997 – February, 2004. Military Service (April, 1999 – June 2001)

PhD DEGREE'S PROJECTS

1. New Gate oxide design for III-V channel devices

- Designed the novel ALD BeO
- ALD BeO precursor synthesis

2. Electrical and Physical Characterization for High-k Gate Dielectrics for MOSFETS

- Measurement of mobility degradation, SILC(Stress Induced Leakage Current), N(P)BTI(Negative or Positive Bias Temperature Instability), HCI(Hot Carrier Injection), TZDB(Time Zero Dielectric Breakdown), TDDB(Time Dependent Dielectric Breakdown), Charge Pumping, Conductance Method, Combined high-low Frequency CV, Split CV

3. III-V MOSFETS Process Developments and Characterization

- Improving and Optimizing process fabrication of III-IV MOSFETS(CAP) such as GaAs, InGaAs, InP and InAs epi substrates
- Surface Passivation technique development and mechanism characterization

4. ReRam Characterization and modeling

- Measurement Forming/Reset/Set with compliance current level
- ITIC Measurement and Characterization, and Its Modeling

WORK EXPERIENCE

Research Associate, Unist, Ulsan, South Korea

Period: July, 2015 – Current

- Graphene
- Superconductor Synthesis

EUV Mask Engineer, Sematech, Albany NY, USA

Period: Feb, 2014 – June, 2015

- Multilayer deposition for Extreme Ultra Violet lithography blank mask.
- Atomic layer controlled Mo/Si and Mo/Be growth for high reflectivity.
- IBD and PVD Mo/Si growth using non-ion beam deposition.
- Mechanism Study of Particle Generation in Magnetron Sputtering.

III-V S/D Contact Engineer, Sematech, Albany NY, USA

Period: Jan, 2012 – Feb, 2013

- S/D metal contact engineering for InGaAs FinFETs.
- S/D and Channel engineering to minimize the contact resistivity.
- P, As and S monolayer doping on Si, Ge and III-V substrates
- sSOI, SiGe, Ge and III-V FinFETs process development and integration.
- Channel & Gate strain engineering development
- Epi channel growth development, optical characterization, epi defect evaluation, and integration.
- Monolayer doping technique development for low S/D contact resistance and low junction depth.
- Flash, Soak, and Microwave annealing for dopant activation and high dielectric quality.

Research Assistant, Department of Electrical Engineering, Univ. Texas at Austin, USA

Period: August, 2006 – 2012. Jan

- High thermal dissipation layer development (ALD BeO) for heat sink and low power devices.
- ReRAM dielectric and metal electrode development, and switching modeling.
- Developing the electronic materials and semiconductor device fabrication processes.
- Characterization and modeling of the thin dielectric breakdown and reliability in high-K gate dielectrics, gate electrode and high-K thin films for semiconductor memory applications.

Intern, Sematech Corporation, Austin, TX

Period: June, 2009 – Dec. 2011

Period: December, 2006 – December, 2007

- New oxide design (ALD BeO)
- Electrical and physical characterization for high-k on Si and high mobility substrates
- ReRAM and TANOS characterization

Research Assistant, Faculty of Electronics and Interconnections

Korea University (within top5 in Korea), Seoul, Korea

Period: January, 2002 - Mar, 2002

- Design and simulation of photonic crystal fiber (PCF) and Coplanar Waveguide (CPW) line
- Modeling and simulating of CPW (coplanar waveguide) and FCPW (Finite Grounded CPW) cross-section

EDUCATIONAL BACKGROUND

Semiconductor Device Physics, Laser electronics, Quantum Mechanics, Quantum magnetism, Si/Ge/III-V doping, Delta doping, Fluid Dynamics, Plasma Physics, Fourier Optics, Adaptive Optics, Thin Film Characterization, Surface Chemistry, Statistical Mechanics, Thermodynamics, Inorganic Chemistry, Organic Chemistry, Lattice Dynamics, Solid State Ionics, Crystallography, Condensed Matter Physics, Nonlinear Optics, Optoelectronics, Superconductor Physics, Low Temperature Physics, Cryogenic Engineering, EUV Mask and Optics, Crystal Physics, Crystal Chemistry, Ceramic Synthesis

COMPUTER SKILLS

Languages: C/C++, JavaScript, HTML

Simulation Tools: Spartan (Quantum Chemistry DFT simulation)

SEMICONDUCTOR SKILLS

Characterization Technique:

MOS CV, IV, Conductance Method, Terman Method, SILC, TDDB,
Transistor characteristics (Id-Vg, Id-Vd), Channel Mobility Estimation by split CV, Dit estimation
by Charge Pumping, Bias-Temperature Instability Measurement, Pulsed Id-Vg

Instrumentation

EDS, XRD, XPS, TEM, SEM, AFM, Cascade probe station, Semiconductor Parameter Analyzer (HP4145, 4156) LCR Meter (HP4194, HP4285), Pulse Generator (HP8115), pA meter/DC voltage source (HP4140), Switch matrix (Si 5010, Agilent E5252) and Digital Oscilloscope (Tektronix TDS3000), Keithly

Device processing:

Mask fabrication, Photolithography, E beam lithography, Thin-film deposition (ALD, sputter, E-beam evaporation, CVD, and PECVD), RIE, Wet etch, RTA, mask layout and fabrication

International Certificate

SCJP(Sun Microsystems Certificated Java Programmer)

Patent

United States Patent. J. H. Yum (1st inventor), “Process for preparing a beryllium oxide layer on a semiconductor substrate” US 20130093029 A1

HONORS & AWARDS

- Sematech Research Award, 2011
- Scholarship, Ministry of electric, information and communication, Korea, 2004 ~ 2006
- Study Scholarship, Korea University, 2002

PUBLICATIONS

- J. H. Yum, H. S. Shin, Ryan M. Mushinski, Todd. W. Hudnall, J. Oh, W. Y. Loh, C. W. Bielawski, G. Bersuker, S. K. Banerjee, W. E. Wang, P.D. Kirsch, and R. Jammy, “A Comparative Study of Gate First and Last Si MOSFETs Fabrication Processes Using ALD Beryllium Oxide as an Interface Passivation Layer“, VLSI Technology, Systems, and Applications (VLSI-TSA), 2013 International Symposium
- J. H. Yum, H. S. Shin, R. Hill, J. Oh, H. D. Lee, Ryan M. Mushinski, Todd. W. Hudnall, C. W. Bielawski, S. K. Banerjee, W. Y. Loh, Wei-E Wang, and Paul Kirsch, “A Study of Capping Layers for Sulfur Monolayer Doping on III-V Junctions“, Appl. Phys. Lett. 101, 253514 (2012)
- J. H. Yum, G. Bersuker, and S. K. Banerjee, “Theoretical Approach Evaluating Beryllium Oxide as A Gate Dielectric In the view points of Electromagnetics and Thermal stability“, Appl. Phys. Lett. 100, 053501 (2012)
- J. H. Yum, G. Bersuker, Todd. W. Hudnall, C. W. Bielawski, P. Kirsch, and S. K. Banerjee, “A Study of Novel ALD Beryllium Oxide as an Interface Passivation Layer for Si MOS Devices“, VLSI Technology, Systems, and Applications (VLSI-TSA), 2012 International Symposium on Volume 1-2
- J. H. Yum, J. Oh, Todd. W. Hudnall, C.W. Bielawski, G. Bersuker, and S. K. Banerjee Comparative Study of SiO₂, Al₂O₃, and BeO “Ultrathin Interfacial Barrier Layers in Si Metal-Oxide-Semiconductor Devices” Active and Passive Electronic Components Volume 2012, Article ID 359580, 7 pages
- J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, Todd. W. Hudnall, G. Bersuker, M. Downer, C. W. Bielawski, J. C. Lee and S. K. Banerjee, “Crystallinity of Atomic Layer Deposited Beryllium Oxide Thin Film and Its Related Electrical and Physical Characteristics on Si and GaAs substrates”, Thin Solid Films 520 (2012) 3091–3095

- J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, Todd. W. Hudnall, G. Bersuker, M. Downer, C. W. Bielawski, J. C. Lee and S. K. Banerjee, "Atomic layer deposited beryllium oxide: Effective passivation layer for III-V metal/oxide/semiconductor devices", *J. Appl. Phys.* 109, 064101 (2011)
- J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, Todd. W. Hudnall, G. Bersuker, M. Downer, C. W. Bielawski, J. C. Lee and S. K. Banerjee, "Inversion Type InP Metal Oxide Semiconductor Field Effect Transistor Using Novel Atomic Layer Deposited BeO Gate Dielectric", *Appl. Phys. Lett.* 99, 033502 (2011)
- J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, Todd. W. Hudnall, M. Downer, C. W. Bielawski, G. Bersuker, J. C. Lee and S. K. Banerjee, "Comparison of Self Cleaning Effect and Electrical Characteristics between Atomic Layer Deposited BeO and Al₂O₃ as an Interface Passivation Layer on GaAs MOS Devices", *J. Vac. Sci. Technol. A* 29(6), Nov/Dec (2011)
- J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, Todd. W. Hudnall, M. Downer, C. W. Bielawski, G. Bersuker, J. C. Lee and S. K. Banerjee. "ALD Beryllium Oxide as a High-k Gate Dielectric for III-V MOS Devices", *International ALD Conference* (2011)
- J. H. Yum, G. Bersuker, T. Akyol, M. Lei, D. A. Ferrer, K.W. Park, Todd. W. Hudnall, M. Downer, C. W. Bielawski, E. T. Yu, J. Price, P. Kirsch, R. Jammy, J. C. Lee and S. K. Banerjee, "ALD BeO: Novel Barrier Layer for High Performance Gate Stacks on Si and High Mobility Substrates", in *IEDM Tech. Dig.*, 2011, pp. 638–641.
- J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, K.W. Park, Todd. W. Hudnall, M. Downer, C. W. Bielawski, G. Bersuker, E. T. Yu, J. Price, J. C. Lee and S. K. Banerjee, "Epitaxial ALD BeO: Efficient Oxygen Diffusion Barrier for EOT Scaling and reliability improvement", *Tran of Electron Device* Vol. 58, No. 12, DEC (2011)
- J. H. Yum, G. Bersuker, T. Akyol, M. Lei, D. A. Ferrer, Todd. W. Hudnall, M. Downer, C. W. Bielawski, J. C. Lee and S. K. Banerjee, "A Study of Highly Crystalline Novel Beryllium Oxide Using Atomic Layer Deposition", *J. Crystal Growth* 334 (2011) 126–133
- D. Koh, J. H. Yum, T. Akyol, D. A. Ferrer, M. Lei, T. W. Hudnall, M. C. Downer, C. W. Bielawski, R. Hill, G. Bersuker, S. K. Banerjee, "Novel atomic layer deposited thin film beryllium oxide for InGaAs MOS Devices" *Indium Phosphide and Related Materials (IPRM)*, 2012 International Conference on 27-30 Aug. 2012
- Ming Lei, J. H. Yum, J. Price, Todd W. Hudnall, C. W. Bielawski, S. K. Banerjee, P. S. Lysaght, G. Bersuker, and M. C. Downer *APPLIED PHYSICS LETTERS* 100, 122906 (2012) "Spectroscopic evaluation of band alignment of atomic layer deposited BeO on Si(100)"
- M. Lei, J. H. Yum, S. K. Banerjee, G. Bersuker, M. C. Downer, *physica status solidi (b)* Volume 249, Issue 6, pages 1160–1165, June 2012, "Band offsets of atomic layer deposited Al₂O₃ and HfO₂ on Si measured by linear and nonlinear internal photoemission"
- Hyoung-Sub Kim, Injo Ok, Manhong Zhang, F. Zhu, S. Park, J. Yum, Han Zhao, and Jack. C. Lee, "Gate oxide scaling down in HfO₂-GaAs metal-oxide-semiconductor capacitor using germanium interfacial passivation layer," *Appl. Phys. Lett.*, Vol. 91, pp. 042904, 2007.
- InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao and Jack C. Lee, "Temperature Effects of Si Interface Passivation Layer Deposition on High-k III-V Metal–Oxide–Semiconductor Characteristics." *Applied physics letters*, 91, 2007.
- Han Zhao, Hyoung-Sub Kim, Feng Zhu, Manhong Zhang, Injo OK, Sung Il Park, Jung Hwan Yum and Jack C Lee, "Metal-oxide-semiconductor capacitors on GaAs with germanium nitride passivation layer", *Applied Physics Letters*, 91, 172101, (2007)
- Sung Il Park, InJo Ok, Hyoung-sub Kim, Feng Zhu, Manhong Zhang, Jung Hwan Yum, Zhao Han, and Jack C. Lee, "Optimization of electrical characteristics of TiO₂-incorporated HfO₂ n-type doped gallium arsenide metal oxide semiconductor capacitor with silicon interface passivation layer", in *Applied Physics Letters* 91, 081908(2007).
- Hyoung-Sub Kim, Injo Ok, Manhong Zhang, F. Zhu, S. Park, J. Yum, Han Zhao, and Jack C. Lee, "Gate oxide scaling down in HfO₂-GaAs metal-oxide-semiconductor capacitor using germanium interfacial passivation layer," *Appl. Phys. Lett.*, Vol. 91, pp. 042904, (2007).

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- Hyoung-Sub Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, J. Oh, P. Majhi, and Jack C. Lee, "Flatband voltage instability characteristics of HfO₂-based GaAs metal-oxidesemiconductor capacitors with a thin Ge layer," *Appl. Phys. Lett.*, Vol. 92, pp. 102904, (2008).
- Hyoung-Sub Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, J. Oh, P. Majhi, and Jack C. Lee, "Inversion-type enhancement-mode HfO₂-based GaAs metal-oxidesemiconductor field effect transistors with a thin Ge layer," *Appl. Phys. Lett.*, Vol. 92, pp. 032907, (2008).
- InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, Domingo Garcia, Prashant Majhi, N. Goel and W. Tsai, C. K. Gaspe, M.B. Santos, and Jack C. Lee, "Metal gate: HfO₂ metal-oxide-semiconductor structures on high-indium-content InGaAs substrate using physical vapor deposition." *Appl. Phys. Lett.* 92, 112904 (2008).
- InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, Domingo Garcia, Prashant Majhi, and Jack C. Lee, "Influence of the substrate orientation on the electrical and material properties of GaAs metal-oxide-semiconductor (MOS) Capacitors and self-aligned transistors using HfO₂ and silicon interface passivation layer (IPL)" *Appl. Phys. Lett.* 92, 1 (2008)
- InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, Domingo Garcia, Prashant Majhi, N. Goel and W. Tsai, C.K. Gaspe, M.B. Santos, and Jack C. Lee, "Self-aligned nchannel metal-oxide-semiconductor field effect transistor on high-indium-content In_{0.53}Ga_{0.47}As and InP using physical vapor deposition HfO₂ and silicon interface passivation Layer." *Appl. Phys. Lett.* 92, 202903 (2008)
- InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao and Jack C. Lee, "Self aligned n-channel GaAs metal-oxide-semiconductor field-effect transistors (MOSFETs) Using HfO₂ and silicon interface passivation layer: post metal annealing optimization." *Microelectronics Engineering* (2008).
- Hyoung-Sub Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, P. Majhi, N. Goel, W. Tsai, C. K. Gaspe, M. B. Santos, and Jack C. Lee, "A study of Metal-OxideSemiconductor Capacitors on GaAs, In_{0.53}Ga_{0.47}As, InAs, and InSb Substrates using a Germanium Interfacial Passivation Layer," *Appl. Phys. Lett.*, (2008).
- Hyoung-Sub Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, P. Majhi, and Jack C. Lee, "HfO₂-based InP n-channel metal-oxide-semiconductor field-effect transistors and metal-oxide-semiconductor capacitors using a germanium interfacial passivation layer," *Appl. Phys. Lett.*, 93, 102906 (2008)
- Han Zhao, Davood Shahrjerdi, Feng Zhu, Manhong Zhang, Hyoung-Sub Kim, Injo OK, Jung Hwan Yum, Sung Il Park, Sanjay K. Banerjee, and Jack C. Lee, "Gate-first inversiontype InP metal-oxide-semiconductor field-effect transistors with atomic-layer-deposited Al₂O₃ gate dielectric", *Applied Physics Letters*, 92, 233508 (2008)
- Han Zhao, Davood Shahrjerdi, Feng Zhu, Hyoung-Sub Kim, Injo OK, Manhong Zhang, Jung Hwan Yum, Sanjay K. Banerjee, and Jack C. Lee, "Inversion-type indium phosphide metal-oxide-semiconductor field-effect transistors with equivalent oxide thickness of 12 Å using stacked HfAlO_x/HfO₂ gate dielectric", *Applied Physics Letters*, 92, 253506 (2008)
- Han Zhao, Davood Shahrjerdi, Feng Zhu, Hyoung-Sub Kim, Injo OK, Manhong Zhang, Jung Hwan Yum, Sanjay K. Banerjee and Jack C Lee, "Inversion-type InP MOSFETs with EOT of 21 Å using atomic layer deposited Al₂O₃ gate dielectric", *Electrochemical and solid-state letters*, 11, H233, (2008)
- Han Zhao, Yen-Ting Chen, Jung Hwan Yum, Niti Goel, Jack C Lee, "Effect of channel doping concentration and thickness on device performance for In_{0.53}Ga_{0.47}As metal-oxidesemiconductor transistors with atomic-layer-deposited Al₂O₃ dielectrics", *Applied Physics Letters*, 94, 093505 (2009)
- Han Zhao, Yen-Ting Chen, Jung Hwan Yum, Yanzhen Wang, Niti Goel, Jack C Lee, "High performance In_{0.7}Ga_{0.3}As metal-oxide-semiconductor transistors with mobility > 4400 cm²/Vs using InP barrier layer", *Applied Physics Letters*, 94, 193502 (2009)

- Han Zhao, Jung Hwan Yum, Yen-Ting Chen, and Jack C Lee, "In_{0.53}Ga_{0.47}As n-MOSFETs with ALD Al₂O₃, HfO₂ and LaAlO₃ gate dielectrics", *Journal of Vacuum Science and Technology B*, 27, 2024, (2009)
- Feng Zhu, Han Zhao, I. Ok, H.S. Kim, M. Zhang, S. Park, J. Yum, Niti Goel, C.K. Gaspe, M.B. Santos, W. Tsai and Jack C. Lee, "Effects of anneal and silicon interface passivation layer thickness on device characteristics of In_{0.53}Ga_{0.47}As n-MOSFETs with HfO₂ gate oxide", *Electrochemical and Solid-State Letters*, 12, H131 (2009)
- Feng Zhu, Han Zhao, I. Ok, H.S. Kim, J. Yum, Niti Goel, C.K. Gaspe, M.B. Santos, W. Tsai, and Jack C. Lee, "A high performance In_{0.53}Ga_{0.47}As Metal-Oxide-Semiconductor Field Effect Transistor with silicon interface passivation layer", *Applied Physics Letters*, 94, 013511 (2009)
- Yen-Ting Chen, Han Zhao, Jung Hwan Yum, Yanzhen Wang, and Jack C. Lee, "Metaloxide-semiconductor field-effect-transistors on indium phosphide using HfO₂ and silicon passivation layer with equivalent oxide thickness of 18Å", *APPLIED PHYSICS LETTERS* 94, 213505, May 2009
- Han Zhao, Yen-Ting Chen, Jung Hwan Yum, Yanzhen Wang, Fei Xue, Fei Zhou, Jack Lee, "High Performance InGaAs MOSFETs with High Mobility using InP Barrier Layer", *Electrochemical Society Transactions*, Vol. 25, Issue #7, p. 397-404 (2009).
- H Zhao, J. Lee, et al, "Effects of gate-first and gate-last process on interface quality of In_{0.53}Ga_{0.47}As metal-oxide-semiconductor capacitors using atomic-layer-deposited Al₂O₃ and HfO₂ oxides", *Applied Physics Letters*, 95, 253501 (2009)
- Yen-Ting Chen, Han Zhao, Jung Hwan Yum, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee "Improved electrical characteristics of TaN/Al₂O₃ / In_{0.53}Ga_{0.47}As metal-oxidesemiconductor field-effect transistors by fluorine incorporation", *APPLIED PHYSICS LETTERS* 95, 013501 (2009)
- Yen-Ting Chen, Han Zhao, Jung Hwan Yum, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "Effects of fluorine incorporation on the electrical properties of atomic-layerdeposited Al₂O₃ gate dielectric on InP substrate", *Journal of The Electrochemical Society*, 157 (3) G71-G75 January (2010)
- InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J Yum, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and Jack C. Lee "Metal Gate – HfO₂ MOS Structures on InGaAs Substrate with Varying Si Interface Passivation Layers and PDA Conditions", *Conference on the Physics and Chemistry of Semiconductor Interfaces*, 2007
- Feng Zhu, Injo Ok, Hyoung-sub Kim, Manhong Zhang, Sung Il Park, Jung Hwan Yum and Jack C. Lee, "Investigation of the passivation mechanism of ultra-thin silicon interface layer for III-V MOS devices," *Conference on the Physics and Chemistry of Semiconductor Interfaces (PCSI)* (2007).
- Hyoung-Sub Kim, Injo Ok, Feng Zhu, M. Zhang, S. Park, J. Yum, H. Zhao, and Jack C. Lee, "n- and p-channel TaN/HfO₂ MOSFETs on GaAs substrate using a germanium interfacial passivation layer," *The 65th annual Device Research Conf.*, pp. 99, 2007.
- Hyoung-Sub Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and Jack C. Lee, "HfO₂-based Metal-Oxide-Semiconductor Capacitors on n-InGaAs Substrate with a Thin Germanium Passivation Layer," *The International Conference on Compound Semiconductor Manufacturing Technology*, pp. 69, 2007.
- InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J Yum, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and Jack C. Lee "Hydrogen Incorporation of Metal Gate HfO₂ MOS Structures on In_{0.2}Ga_{0.8}As Substrate with Si Interface Passivation Layer", *International Conference on Compound Semiconductor Manufacturing Technology*, 2007.
- InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J Yum, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and Jack C. Lee, "Metal Gate HfO₂ MOS Structures on InGaAs Substrate with Varying Si Interface Passivation Layer and PDA Condition," *J. Vac. Sci. Technol. B* 25, Jul/Aug 2007.
- Injo Ok, Hyung-sub Kim, Manhong Zhang, Feng Zhu, Sung-il Park, Junghwan Yum, Han Zhao and Jack C. Lee, "Post Metal Annealing Optimization of Self-Aligned n- channel GaAs MOSFETs Using HfO₂ and Silicon Interface Passivation Layer," *the International Symposium on Advanced Gate Stack Technology*, September 2007.

- InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, Domingo Garcia, Prashant Majhi, and Jack C. Lee, "Influence of the substrate orientation on the electrical and material properties of GaAs MOSFETs Using HfO₂ and Silicon Interface Passivation Layer," Semiconductor Interface Specialists Conference (SISC), December 2007.
- InJo Ok, H. Kim, M. Zhang, F. Zhu, H. Zhao, S. Park, J. Yum, Domingo Garcia, Prashant Majhi, N. Goel and W. Tsai, C.K. Gaspe, M.B. Santos, and Jack C. Lee, "Self-Aligned nchannel MOSFET on InP and In_{0.53}Ga_{0.47}As Using Physical Vapor Deposition HfO₂ and Silicon Interface Passivation Layer." IEEE Device Research Conference, June 2008.
- Feng Zhu, InJo Ok, Hyoung-sub Kim, Manhong Zhang, Sung Il Park, Jung Hwan Yum, Han Zhao and Jack C. Lee, "Can GaAs MOS device match with its silicon counterpart in interface quality by using silicon interface passivation layer and HfO₂ gate oxide?" Electronic Materials Conference (EMC) (2008).
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- Feng Zhu, Han Zhao, H.S. Kim, I. Ok, J. Yum and Jack C. Lee, "The effects of silicon interface passivation layer thickness on device characteristics of InP enhancement-mode nMOSFETs with HfO₂ gate oxide", IEEE SISC Semiconductor Interface Specialists Conference 2008
- Feng Zhu, Han Zhao, H.S. Kim, I. Ok, J. Yum and Jack C. Lee, "A high performance enhancement-mode In_{0.53}Ga_{0.47}As nMOSFET with directly sputtered HfO₂ gate oxide", IEEE SISC Semiconductor Interface Specialists Conference 2008
- H. Zhao, D. Shahrjerdi, F. Zhu, H.S. Kim, J. Yum, S. Banerjee and J. C. Lee "Atomic-layerdeposited Al₂O₃ gate dielectrics on InP using sulfur passivation", 50th Electronic Materials Conference, (2008)
- H. Zhao, D. Shahrjerdi, F. Zhu, H.S. Kim, J. Yum, S. Banerjee and J. C. Lee "Atomic-layerdeposited Al₂O₃ gate dielectrics on InP using sulfur passivation", 50th Electronic Materials Conference, (2008)
- H. Zhao, Y. Chen, J. Yum, Y. Wang, N. Goel, S. Kovesnikov, W. Tsai, and J. C. Lee, "HfO₂-Based In_{0.53}Ga_{0.47}As MOSFETs (EOT≈10Å) Using Various Interfacial Dielectric Layers", IEEE Device Research Conference, (2009)
- Han Zhao, Jung Hwan Yum, Yen-Ting Chen, and Jack C Lee "In_{0.53}Ga_{0.47}As n-MOSFETs with ALD Al₂O₃, HfO₂ and LaAlO₃ gate dielectrics", 36th Conference on the Physics and Chemistry of Semiconductor Interfaces, (2009)
- Yen-Ting Chen, Han Zhao, Jung Hwan Yum, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "In_{0.53}Ga_{0.47}As MOSFETs with CF₄ plasma treatment and Al₂O₃ gate oxide", International Symposium on Advanced Gate Stack Technology (ISAGST), August 2009
- Yen-Ting Chen, Han Zhao, Jung Hwan Yum, Yanzhen Wang, and Jack C. Lee, "Atomic layer deposited HfO₂ gate dielectrics on InP using silicon interface passivation layer "Electronic Materials Conference (EMC) 2009
- Han Zhao, Yen-Ting Chen, Jung Hwan Yum, and Jack C Lee "Channel Doping Concentration and Thickness Dependence of Device Performance for In_{0.53}Ga_{0.47}As n-MOSFETs with ALD Al₂O₃ dielectrics", 2009 Materials Research Society Spring Meeting
- J. Lee, H. Zhao, Y. Chen, J. Yum, F. Xue, F. Zhou and Y. Wang, (Invited Paper) "High Performance InGaAs MOSFETs with High Mobility using InP Barrier Layer" 216th Electrochemical Society Meeting (E10 - ULSI Process Integration) in Vienna, Austria, October 2009.
- H. Zhao, N. Goel, J. Huang, Y. Chen, J. Yum, Y. Wang, F. Zhou, F. Xue, and J. Lee, "Factors Enhancing In_{0.7}Ga_{0.3}As MOSFETs and Tunneling FETs Device performance" IEEE Device Research Conference, (2010).

Around 74 journals and conferences as an author or co-author.